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Fault-Tolerance Techniques for SRAM-based FPGAs



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Fault Tolerance Techniques For Sram Based Fpgas Frontiers In Electronic Testing

Kanad Chakraborty, Pinaki Mazumder



Fault Tolerance Techniques For Sram Based Fpgas Frontiers In Electronic Testing:

Fault-Tolerance Techniques for SRAM-Based FPGAs Fernanda Lima Kastensmidt, Ricardo Reis, 2007-02-01 Fault tolerance in integrated circuits is not an exclusive concern regarding space designers or highly reliable application engineers. Rather designers of next generation products must cope with reduced margin noises due to technological advances. The continuous evolution of the fabrication technology process of semiconductor components in terms of transistor geometry shrinking power supply speed and logic density has significantly reduced the reliability of very deep submicron integrated circuits in face of the various internal and external sources of noise. The very popular Field Programmable Gate Arrays customizable by SRAM cells are a consequence of the integrated circuit evolution with millions of memory cells to implement the logic embedded memories routing and more recently with embedded microprocessors cores. These re programmable systems on chip platforms must be fault tolerant to cope with present days requirements. This book discusses fault tolerance techniques for SRAM based Field Programmable Gate Arrays FPGAs. It starts by showing the model of the problem and the upset effects in the programmable architecture. In the sequence it shows the main fault tolerance techniques used nowadays to protect integrated circuits against errors. A large set of methods for designing fault tolerance systems in SRAM based FPGAs is described. Some presented techniques are based on developing a new fault tolerant architecture with new robustness FPGA elements. Other techniques are based on protecting the high level hardware description before the synthesis in the FPGA. The reader has the flexibility of choosing the most suitable fault tolerance technique for its project and to compare a set of fault tolerant techniques for programmable logic applications. **FPGAs and Parallel Architectures**

for Aerospace Applications Fernanda Kastensmidt, Paolo Rech, 2015-12-07 This book introduces the concepts of soft errors in FPGAs as well as the motivation for using commercial off the shelf COTS FPGAs in mission critical and remote applications such as aerospace. The authors describe the effects of radiation in FPGAs present a large set of soft error mitigation techniques that can be applied in these circuits as well as methods for qualifying these circuits under radiation. Coverage includes radiation effects in FPGAs fault tolerant techniques for FPGAs use of COTS FPGAs in aerospace applications experimental data of FPGAs under radiation FPGA embedded processors under radiation and fault injection in FPGAs. Since dedicated parallel processing architectures such as GPUs have become more desirable in aerospace applications due to high computational power GPU analysis under radiation is also discussed. **New Methods of Concurrent Checking**

Michael Gössel, Vitaly Ocheretny, Egor Sogomonyan, Daniel Marienfeld, 2008-04-26 Computers are everywhere around us. We for example as air passengers car drivers laptop users with Internet connection cell phone owners hospital patients inhabitants in the vicinity of a nuclear power station students in a digital library or customers in a supermarket are dependent on their correct operation. Computers are incredibly fast inexpensive and equipped with almost unimaginable large storage capacity. Up to 100 million transistors per chip are quite common today a single transistor for each citizen of a large capital city in the

world can be easily accommodated on an ordinary chip. The size of such a chip is less than 1 cm. This is a fantastic achievement for an unbelievably low price. However, the very small and rapidly decreasing dimensions of the transistors and their connections over the years are also the reason for growing problems with reliability that will dramatically increase for the nano technologies in the near future. Can we always trust computers? Are computers always reliable? Are chips sufficiently tested with respect to all possible permanent faults if we buy them at a low price or have errors due to undetected permanent faults to be discovered by current checking? Besides permanent faults, many temporary or transient faults are also to be expected.

Embedded Systems Krzysztof Iniewski, 2012-10-26. Covers the significant embedded computing technologies highlighting their applications in wireless communication and computing power. An embedded system is a computer system designed for specific control functions within a larger system, often with real-time computing constraints. It is embedded as part of a complete device, often including hardware and mechanical parts. Presented in three parts: Embedded Systems, Hardware Design and Implementation provides readers with an immersive introduction to this rapidly growing segment of the computer industry. Acknowledging the fact that embedded systems control many of today's most common devices such as smart phones, PC tablets, as well as hardware embedded in cars, TVs, and even refrigerators and heating systems, the book starts with a basic introduction to embedded computing systems. It hones in on system-on-a-chip (SoC), multiprocessor system-on-chip (MPSoC), and network-on-chip (NoC). It then covers on-chip integration of software and custom hardware accelerators, as well as fabric flexibility, custom architectures, and the multiple I/O standards that facilitate PCB integration. Next, it focuses on the technologies associated with embedded computing systems, going over the basics of field-programmable gate array (FPGA), digital signal processing (DSP), and application-specific integrated circuit (ASIC) technology, architectural support for on-chip integration of custom accelerators with processors, and OS support for these systems. Finally, it offers full details on architecture, testability, and computer-aided design (CAD) support for embedded systems, soft processors, heterogeneous resources, and on-chip storage, before concluding with coverage of software support, in particular OS Linux. *Embedded Systems: Hardware Design and Implementation* is an ideal book for design engineers looking to optimize and reduce the size and cost of embedded system products and increase their reliability and performance.

Biologically-Inspired Collaborative Computing Mike Hinchey, Anastasia Pagnoni, Franz J. Rammig, Hartmut Schmeck. Look deep into nature and you will understand everything better, advised Albert Einstein. In recent years, the research communities in Computer Science, Engineering, and other disciplines have taken this message to heart, and a relatively new field of biologically inspired computing has been born. Inspiration is being drawn from nature, from the behaviors of colonies of ants, of swarms of bees, and even the human body. This new paradigm in computing takes many simple autonomous objects or agents and lets them jointly perform a complex task without having the need for centralized control. In this paradigm, these simple objects interact locally with their environment using simple rules. Applications include optimization algorithms, communications networks, scheduling

and decision making supply chain management and robotics to name just a few There are many disciplines involved in making such systems work from artificial intelligence to energy aware systems Often these disciplines have their own field of focus have their own conferences or only deal with specialized problems e.g. swarm intelligence biologically inspired computation sensor networks The Second IFIP Conference on Biologically Inspired Collaborative Computing aims to bridge this separation of the scientific community and bring together researchers in the fields of Organic Computing Autonomic Computing Self Organizing Systems Pervasive Computing and related areas We are very pleased to have two very important keynote presentations *Swarm Robotics The Coordination of Robots via Swarm Intelligence Principles* by Marco Dorigo, Université Libre de Bruxelles, Belgium, of which an abstract is included in this volume

On-Chip Current Sensors for Reliable, Secure, and Low-Power Integrated Circuits Rodrigo Possamai Bastos, Frank Sill Torres, 2019-09-30 This book provides readers with insight into an alternative approach for enhancing the reliability security and low power features of integrated circuit designs related to transient faults hardware Trojans and power consumption The authors explain how the addition of integrated sensors enables the detection of ionizing particles and how this information can be processed at a high layer The discussion also includes a variety of applications such as the detection of hardware Trojans and fault attacks and how sensors can operate to provide different body bias levels and reduce power costs Readers can benefit from these sensors based approaches through designs with fast response time non intrusive integration on gate level and reasonable design costs

Oscillation-Based Test in Mixed-Signal Circuits Gloria Huertas Sánchez, Diego Vázquez García de la Vega, Adoración Rueda Rueda, Jose Luis Huertas Díaz, 2007-06-03 *Oscillation Based Test in Mixed Signal Circuits* presents the development and experimental validation of the structural test strategy called Oscillation Based Test (OBT) in short The results here presented allow to assert not only from a theoretical point of view but also based on a wide experimental support that OBT is an efficient defect oriented test solution complementing the existing functional test techniques for mixed signal circuits

Design and Test Technology for Dependable Systems-on-Chip Ubar, Raimund, Raik, Jaan, Vierhaus, Heinrich Theodor, 2010-12-31 This book covers aspects of system design and efficient modelling and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip (SoC) Multi Processor System on Chip (MPSoC) or Network on Chip (NoC)

Proceedings, 2006 **SBCCI 2006**, 2006 **The British National**

Bibliography Arthur James Wells, 2006 [Index to IEEE Publications](#) Institute of Electrical and Electronics Engineers, 1994

Hybrid Fault Tolerance Techniques to Detect Transient Faults in Embedded Processors José Rodrigo Azambuja, Fernanda Kastensmidt, Jürgen Becker, 2014-07-07 This book describes fault tolerance techniques based on software and hardware to create hybrid techniques They are able to reduce overall performance degradation and increase error detection when associated with applications implemented in embedded processors Coverage begins with an extensive discussion of the current state of the art in fault tolerance techniques The authors then discuss the best trade off between software based and

hardware based techniques and introduce novel hybrid techniques Proposed techniques increase existing fault detection rates up to 100% while maintaining low performance overheads in area and application execution time

Fault Injection Techniques and Tools for Embedded Systems Reliability Evaluation Alfredo Benso, Paolo Prinetto (ed.), 2003-10-31 Our society is faced with an increasing dependence on computing systems not only in high tech consumer applications but also in areas e g air and railway traffic control nuclear plant control aircraft and car control where a failure can be critical for the safety of human beings Unfortunately it is accepted that large digital systems cannot be fault free Some faults may be attributed to inaccuracy during the development while others can come from external causes such as environmental stress Radiations electromagnetic interference and power glitches are some of the most common causes of transient faults As a consequence the past years have seen a growing interest in methods for studying the behaviour of computer based systems when faults occur and several approaches have been proposed to evaluate the dependability properties of a computer based system Fault Injection i e the artificial injection of faults into a computer system in order to study its behaviour emerged as a viable solution and has been deeply investigated by both academia and industry Different techniques have been proposed and some of them practically experimented Fault Injection Techniques and Tools for Embedded Systems Reliability Evaluation intends to be a comprehensive guide to Fault Injection techniques used to evaluate the dependability of a digital system The description and the critical analysis of different Fault Injection techniques and tools will be authored by key scientists in the field of system dependability and fault tolerance

Fault-Tolerance Techniques for Spacecraft Control Computers Mengfei Yang, Gengxin Hua, Yanjun Feng, Jian Gong, 2017-01-23 Comprehensive coverage of all aspects of space application oriented fault tolerance techniques Experienced expert author working on fault tolerance for Chinese space program for almost three decades Initiatively provides a systematic texts for the cutting edge fault tolerance techniques in spacecraft control computer with emphasis on practical engineering knowledge Presents fundamental and advanced theories and technologies in a logical and easy to understand manner Beneficial to readers inside and outside the area of space applications

Fault-tolerance and Reliability Techniques for High-density Random-access Memories Kanad Chakraborty, Pinaki Mazumder, 2002 This book deals with primarily with reliable and fault tolerant circuit design and evaluation techniques for RAMS It examines both the manufacturing fault tolerance e g self repair at the time of manufacturing and online and field related fault tolerance e g error correction It talks a lot about important techniques and requirements and explains what needs to be done and why for each of the techniques

Detection of Configuration Memory Upsets Causing Persistent Errors in SRAM-based FPGAs, 2004 FPGA designers are becoming increasingly aware of fault tolerance issues in modern FPGA designs especially designs destined for a radiation environment We classify errors due to upsets within the configuration bitstream into two categories namely persistent and non persistent Persistent errors generally cannot be tolerated However non persistent errors can be tolerated in certain types of designs as long as they are properly accounted for We discuss situations in which nonpersistent

errors are acceptable and describe a technique for the detection of upsets causing persistent errors within the configuration memory of an SRAM based FPGA

Reconfigurable Fault Tolerance for Space Systems Adam M. Jacobs, 2013 Second low overhead fault tolerance techniques which can be used within the RFT framework for improved performance must be investigated The effectiveness of Algorithm Based Fault Tolerance ABFT for FPGA based systems is explored for matrix multiplication and FFT ABFT kernels were developed for an FPGA platform and reliability was measured using fault injection testing We show that matrix multiplication and FFTs with ABFT can provide improved reliability vulnerability reduced by 98% with low resource overhead and scale favorably with additional parallelism Third methods for facilitating the integration of RFT hardware into existing PR based systems and architectures are explored We expand the RFT framework to be used with bus based or point to point architectures We design a fault tolerant task scheduling algorithm which can schedule RFT tasks in a dynamically changing fault environment in order to maximize system performability Combined these three areas demonstrate the capability of RFT to provide both performance and reliability in space Using low overhead fault tolerance techniques and reconfiguration RFT can meet the strict constraints of next generation space systems

A Comprehensive Comparison Between Design for Testability Techniques for Total Dose Testing of Flash-based FPGAs Mohamed Ayman Ahmed Ibrahim, 2019 Abstract Radiation sources exist in different kinds of environments where electronic devices often operate Correct device operation is usually affected negatively by radiation The radiation resultant effect manifests in several forms depending on the operating environment of the device like total ionizing dose effect TID or single event effects SEEs such as single event upset SEU single event gate rupture SEGR and single event latch up SEL CMOS circuits and Floating gate MOS circuits suffer from an increase in the delay and the leakage current due to TID effect This may damage the proper operation of the integrated circuit Exhaustive testing is needed for devices operating in harsh conditions like space and military applications to ensure correct operations in the worst circumstances The use of worst case test vectors WCTVs for testing is strongly recommended by MIL STD 883 method 1019 which is the standard describing the procedure for testing electronic devices under radiation However the difficulty of generating these test vectors hinders their use in radiation testing Testing digital circuits in the industry is usually done nowadays using design for testability DFT techniques as they are very mature and can be relied on DFT techniques include but not limited to ad hoc technique built in self test BIST muxed D scan clocked scan and enhanced scan DFT is usually used with automatic test patterns generation ATPG software to generate test vectors to test application specific integrated circuits ASICs especially with sequential circuits against faults like stuck at faults and path delay faults Despite all these recommendations for DFT radiation testing has not benefited from this reliable technology yet Also with the big variation in the DFT techniques choosing the right technique is the bottleneck to achieve the best results for TID testing In this thesis a comprehensive comparison between different DFT techniques for TID testing of flash based FPGAs is made to help designers choose the best suitable DFT technique depending

on their application The comparison includes muxed D scan technique clocked scan technique and enhanced scan technique The comparison is done using ISCAS 89 benchmarks circuits Points of comparisons include FPGA resources utilization difficulty of designs bring up added delay by DFT logic and robust testable paths in each technique Software Fault Tolerance Michael R. Lyu, 1995-05-09 Software fault tolerance techniques involve error detection exception handling monitoring mechanisms and error recovery This issue of Trends in Software focuses on identification formulation application and evaluation of current software fault tolerance techniques

The Enigmatic Realm of **Fault Tolerance Techniques For Sram Based Fpgas Frontiers In Electronic Testing**: Unleashing the Language is Inner Magic

In a fast-paced digital era where connections and knowledge intertwine, the enigmatic realm of language reveals its inherent magic. Its capacity to stir emotions, ignite contemplation, and catalyze profound transformations is nothing short of extraordinary. Within the captivating pages of **Fault Tolerance Techniques For Sram Based Fpgas Frontiers In Electronic Testing** a literary masterpiece penned with a renowned author, readers embark on a transformative journey, unlocking the secrets and untapped potential embedded within each word. In this evaluation, we shall explore the book's core themes, assess its distinct writing style, and delve into its lasting affect the hearts and minds of people who partake in its reading experience.

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